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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,475	02/01/2002	Edward Colles Nevill	1103179-0009	5943

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WHITE & CASE LLP
PATENT DEPARTMENT
1155 AVENUE OF THE AMERICAS
NEW YORK, NY 10036

EXAMINER	
COULTER, KENNETH R	
ART UNIT	PAPER NUMBER
2445	

MAIL DATE	DELIVERY MODE
12/30/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/066,475	NEVILL, EDWARD COLLES	
	Examiner	Art Unit	
	Kenneth R. Coulter	2445	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-64 and 66-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-14* is/are allowed.

6)☒ Claim(s) *15-64 and 66-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/477,781.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 64 and 66 – 70 are currently under consideration in the present Application.

Reissue Applications

Applicant is reminded of the continuing obligation under 37 CFR 1.178(b), to timely apprise the Office of any prior or concurrent proceeding in which Patent No. 6,021,265 is or was involved. These proceedings would include interferences, reissues, reexaminations, and litigation.

Applicant is further reminded of the continuing obligation under 37 CFR 1.56, to timely apprise the Office of any information which is material to patentability of the claims under consideration in this reissue application.

These obligations rest with each individual associated with the filing and prosecution of this application for reissue. See also MPEP §§ 1404, 1442.01 and 1442.04.

Claim Objections

Claims 51 – 56 are objected to because of the following informalities: "bythe" (claim 51, line 12). Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 57 – 64 are rejected under 35 USC 112, second paragraph.

Claim 57 recites the limitation "a second instruction" in line 13. The phrase "a second instruction" was previously referenced in line 7 of claim 57.

There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 15 – 64 and 66 – 70 are rejected under 35 U.S.C. 102(b) as being anticipated by Larsen (U.S. Pat. No. 5,115,500) (Plural Incompatible Instruction Format Decode Method and Apparatus).

2.1 Regarding claim 15, Larsen discloses a method of switching between a predetermined plurality of instruction sets used by a data processing apparatus, the method comprising:

in response to a first instruction:

accessing a sequence of bits, the sequence of bits having an address portion that identifies the location of a second instruction in a memory and an instruction set indicator portion (Fig. 2, items 3, 10, 2 (***the bits that are not the top 3 bits from the IAR***); col. 5, line 34 – col. 6, line 2);

identifying an instruction set selected from the predetermined plurality of instruction sets based on the instruction set indicator portion of the sequence of bits (Fig. 2; col. 5, line 52 – col. 6, line 16; col. 7, lines 12 – 37);

setting one or more control flags to indicate that a current instruction set for the data processing apparatus is the instruction set identified based on the instruction set indicator portion of the sequence of bits (Fig. 2; col. 5, line 52 – col. 6, line 16; col. 7, lines 12 – 37); and

retrieving the second instruction from the location specified by the address portion of the sequence of bits (Fig. 2; col. 5, line 52 – col. 6, line 16; col. 7, lines 12 – 37),

wherein the instruction set identified by the instruction set portion of the sequence of bits is identifiable without regard to the address specified by the address portion of the sequence of bits (Fig. 2, items 3, 10, 2 (***the bits that are the top 3 bits from the IAR***); col. 5, line 34 – col. 6, line 2).

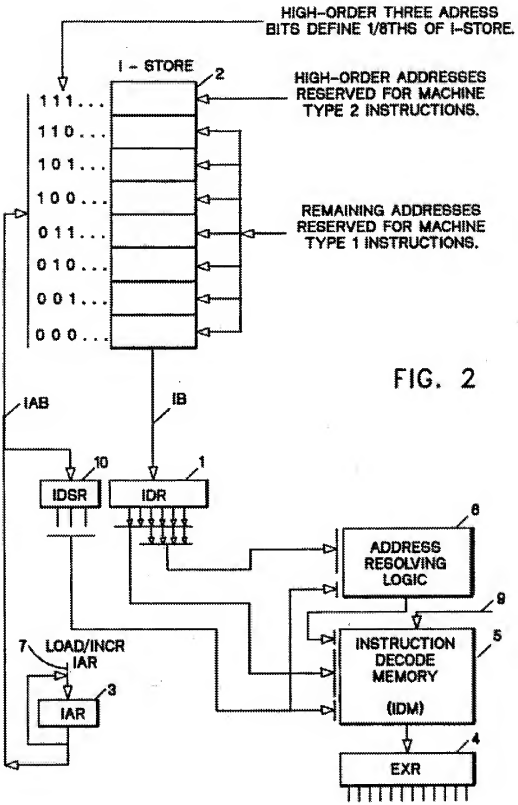

HIGH-ORDER THREE ADRESS BITS DEFINE 1/8THS OF I-STORE.
I - STORE
2
111...
110...
101...
100...
011...
010...
001...
000...
HIGH-ORDER ADDRESSES RESERVED FOR MACHINE TYPE 2 INSTRUCTIONS.
REMAINING ADDRESSES RESERVED FOR MACHINE TYPE 1 INSTRUCTIONS.
IAB
IB
10
1
IDSR
IDR
6
ADDRESS RESOLVING LOGIC
9
7
LOAD/INCR IAR
3
IAR
INSTRUCTION DECODE MEMORY
(IDM)
5
4
EXR

FIG. 2

Col. 5, line 52 – col. 6, line 16 of Larsen

FIG. 2 illustrates the addition of a new component, the Instruction Decode Selection Register, IDSR, 10. This element is a register that is operated so that it retains the instruction address or some portion thereof of the instruction currently residing in IDR 1. The IDSR 10 is used to trap or retain the address of the last instruction that was fetched from I-store 2. The IDSR 10 retains a portion of the address of the last instruction fetched and will be clocked with the same signal that causes the IDR 1 to be loaded. The retained portion may be all of the address or less if required. Thus, it will always receive **the address of the instruction that is loaded into the IDR 1. In FIG. 2, IDSR 10 is assumed to contain only the high order three bits from the IAR 3** because of the arbitrarily assumed partitioning of I-store 2 in the instant example. **Only the three high order bits necessary to define which of the eight equal arbitrary segments of I-store or partitions are being addressed.**

The contents of IDSR 10 and of IDR 1 are taken together in FIG. 2 to provide a look-up address within the IDM 5. Only specific portions of the undecoded instruction in IDR may be needed according to the format of the instruction being fetched. The other portion of the input address to the IDM 5 is the output from the IDSR 10 which identifies the fetched-from address in I-store 2, or in the instant example, at least the range in which the address lies within I-store 2. Decoding of any specific instruction in the IDR 1 thus depends not only on the contents of the IDR 1 but on the region of the I-store 2 from which the instruction was fetched. This portion of the address is provided by the IDSR 10 output.

Col. 5, line 34 – col. 6, line 2 of Larsen

FIG. 2 illustrates a block diagram of the major portions of the logic required to accommodate the changes proposed by the preferred embodiment of this invention. The logic shown is similar to that in FIG. 1, but omits the ILR 8 and its loading line 7 for simplicity and includes only the elements necessary for implementing the multiple instruction type decoding of the present invention. In addition, FIG. 2 shows an example of the instruction store 2 with partitioning illustrated for accommodating two types of different, incompatible format machine language instructions. As illustrated, the high order addresses have been arbitrarily reserved for machine type or format 2 instructions. These are identified as having the high order address

beginning with 111 in binary and reserve 1/8 of the instruction store total capacity for machine type 2 instructions. The remaining addresses are arbitrarily reserved for machine type 1 instructions as illustrated.

FIG. 2 illustrates the addition of a new component, the Instruction Decode Selection Register, IDSR, 10. This element is a register that is operated so that it retains the instruction address or some portion thereof of the instruction currently residing in IDR 1. The IDSR 10 is used to trap or retain the address of the last instruction that was fetched from I-store 2. The IDSR 10 retains a portion of the address of the last instruction fetched and will be clocked with the same signal that causes the IDR 1 to be loaded. The retained portion may be all of the address or less if required. Thus, it will always receive the address of the instruction that is loaded into the IDR 1. In FIG. 2, **IDSR 10 is assumed to contain only the high order three bits from the IAR 3** because of the arbitrarily assumed partitioning of I-store 2 in the instant example. **Only the three high order bits necessary to define which of the eight equal arbitrary segments of I-store or partitions are being addressed.**

2.2 Per claim 16, Larsen teaches the method of claim 15, further comprising executing the second instruction as an instruction of the current instruction set (Fig. 2, items 10, 5, 4; col. 5, line 34 – col. 6, line 2).

2.3 Regarding claim 17, Larsen discloses the method of claim 15 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X (Abstract; Fig. 2; col. 6, lines 41 – 66).

2.4 Per claim 18, Larsen teaches the method of claim 17 wherein Y is 16 (Abstract; Fig. 2; col. 6, lines 41 – 66 "execute also 'type 2' format or language instructions that arbitrarily utilize **16 bit words** ...").

However, Larsen does not explicitly disclose that X is a **32 bit** instruction word.

Larsen does teach "**let us suppose** that a 'type 1' format or language instruction set requires **24 bit words** ..." (col. 6, lines 41 – 42).

Clearly, it would have been inherent for the 24 bit word example chosen in Larsen to be substituted with a 32 bit word example.

2.5 Regarding claim 19, Larsen discloses the method of claim 15 wherein the instruction set indicator portion of the sequence of bits comprises one or more **least** significant bits of the sequence of bits (Fig. 2, items 10, 5, 4; col. 5, line 34 – col. 6, line 2).

2.6 Per claim 20, Larsen teaches the method of claim 15 wherein the instruction set indicator portion of the sequence of bits comprises one or more **most** significant bits of the sequence of bits (Fig. 2, items 10, 5, 4; col. 5, line 34 – col. 6, line 2).

2.7 Regarding claims 21 – 26, the rejection of claims 15 – 20 under 35 USC 102(b) (paragraphs 2.1 - 2.6 above) applies fully.

2.8 Regarding claim 66, Larsen discloses a method of selecting an instruction set comprising the steps of:

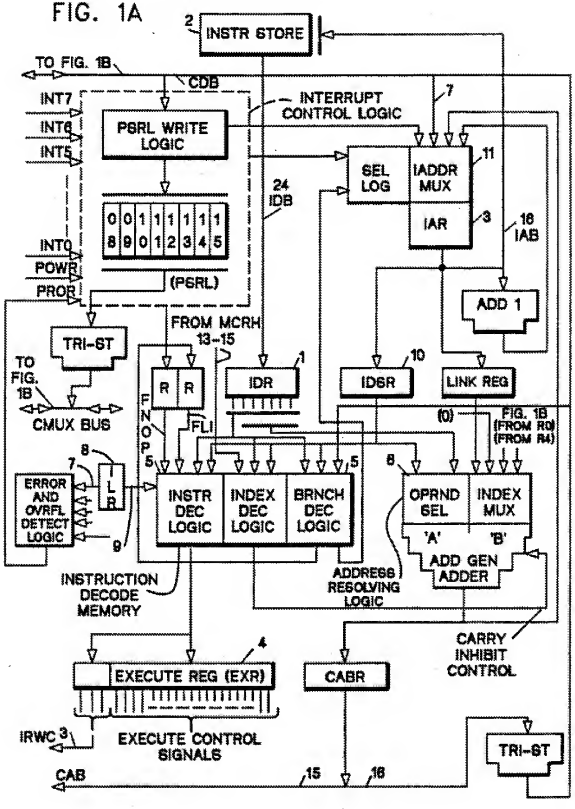
receiving a branching instruction written in a first instruction set of a plurality of instruction sets (Fig. 1A, item 5 "**BRNCH DEC LOGIC**"; Figs. 1A, items 1, 3; Fig. 2; col. 4, line 56 – col. 5, line 12 "a single program which may consist of process instructions or entire **sub-routines** or code modules from dissimilar machines and in dissimilar or incompatible formats …"; col. 5, line 34 – col. 6, line 2; col. 7, lines 12 – 37);

in response to the branching instruction, inserting an address of a second instruction, which specifies the location of the second instruction in a memory, into a register and setting the value of a flag, where the value of the flag is not dependent upon the address of the location of the second instruction in the memory (Figs. 1A, 2; col. 5, line 52 – col. 6, line 16; col. 7, lines 12 – 37 "IDR 1 and IDSR 10 will be loaded with the **next instruction to be decoded** and the address in I-store from which it was fetched, respectively.");

selecting an instruction set based upon the value of the flag (Fig. 2; col. 5, line 52 – col. 6, line 16; col. 7, lines 12 – 37); and

acquiring the next instruction at the address inserted into the register (Fig. 2; col. 5, line 52 – col. 6, line 16; col. 7, lines 12 – 37).

FIG. 1A


2
INSTR STORE
TO FIG. 1B
CDB
INT7
INT6
INT5
INT0
POWR
PROR
PSRL WRITE LOGIC
INTERRUPT CONTROL LOGIC
7
SEL LOG
IADDR MUX
11
IAR
3
16 IAB
24 IDB
0 0 1 1 1 1 1 1
8 9 0 1 2 3 4 5
(PSRL)
ADD 1
FROM MCRH 13-15
TRI-ST
TO FIG. 1B
CMUX BUS
R R
IDR
1
IDBR
10
LINK REG
FNOP
FLI
(0)
FIG. 1B (FROM R0) (FROM R4)
8
7
5
5
8
ERROR AND OVRFL DETECT LOGIC
L R
9
INSTR DEC LOGIC
INDEX DEC LOGIC
BRNCH DEC LOGIC
OPRND SEL
INDEX MUX
'A'
'B'
ADD GEN ADDER
INSTRUCTION DECODE MEMORY
ADDRESS RESOLVING LOGIC
CARRY INHIBIT CONTROL
4
EXECUTE REG (EXR)
CABR
IRWC 3
EXECUTE CONTROL SIGNALS
TRI-ST
CAB
15
16

2.9 Per claim 67, Larsen teaches a processing apparatus comprising:

a pointer for identifying an address of a next instruction that is written in a first instruction set of a plurality of instruction sets (Fig. 2; col. 5, line 52 – col. 6, line 16; col. 7, lines 12 – 37); and

a flag for identifying the first instruction set (Fig. 2; col. 5, line 52 – col. 6, line 16; col. 7, lines 12 – 37);

wherein:

the pointer and the flag are both written in response to an instruction from a second instruction set of the plurality of instruction sets (Fig. 2; col. 5, line 52 – col. 6, line 16; col. 7, lines 12 – 37), and

the value of the flag is not dependent upon **the address that specifies the location in the memory of the next instruction** (Fig. 2; col. 5, line 52 – col. 6, line 16; col. 7, lines 12 – 37).

2.10 Regarding claim 68, Larsen discloses the apparatus of claim 67 wherein:

the first instruction set is different from the second instruction set (Abstract; Fig. 2).

2.11 Per claim 69, Larsen teaches the apparatus of claim 67 wherein:

the pointer and the flag are located in a single register (Fig. 2; col. 7, lines 12 – 37).

2.12 Regarding claim 70, Larsen discloses the apparatus of claim 67 wherein:

the pointer and the flag are not located in a single register, yet are written to as if portions of a single register (Fig. 2; col. 5, line 52 – col. 6, line 16; col. 7, lines 12 – 37).

2.13 Per claims 27 – 64, the rejection of claims 15 – 26 and 66 – 70 under 35 USC 102(b) (paragraphs 2.1 – 2.12 above) applies fully.

Response to Arguments

Applicant argues that in view "of the rejoining of all the claims in the instant application, Applicant submits that the reissue declaration is not defective as it addresses errors to be corrected by the addition of claims 15-64 and 66-70 to the patent upon reissue."

Examiner agrees.

The rejection of the reissue oath has been withdrawn.

Claims 1 – 64 and 66 – 70 are currently under consideration in the present Application.

Allowable Subject Matter

Claims 1 – 14 are allowed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth R. Coulter whose telephone number is 571 272-3879. The examiner can normally be reached on M - F, 7:30 am - 4 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew T. Caldwell can be reached on 571 272-3868. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth R Coulter/
Primary Examiner, Art Unit 2445

/KRC/